UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/662,832	09/15/2000	Timothy J. van Hook	1778.0100002	2552

7590 08/08/2005

STERNE KESSLER GOLDSTEIN & FOX PLLC
1100 NEW YORK AVENUE N W
SUITE 600
WASHINGTON, DC 20005-3934

EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 08/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/662,832	VAN HOOK ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 49-64* is/are pending in the application.

4a) Of the above claim(s) *2-48* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 49-64* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/08/03, 09/03/02*, 08/22/02
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Clams 1,49-64 are presented for examination. Claims 2-48 have been canceled.

2. Applicant is kindly suggested in the next response to provide copies of page 1 and page 2 of the IDS filed on May 22, 2002, which were apparently missing from the file record.

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claim 49 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The reasons are given below.

4. As to claim 49, The language of the claim raises a question as to whether the claim is directed merely to an abstract idea that is not tied to a technological art, environment or machine which would result in practical application producing a concrete, useful, and tangible result to form the basis of statutory subject matter under 35 U.S.C. 101. The claim recites producing target vector for SIMD processing , however, no SIMD implementation has been found in the claim. Furthermore, the source vectors are non-functional descriptive material. When nonfunctional descriptive material is recorded on some computer-readable medium, it is not statutory since no requisite functionality is present to satisfy the practical application requirement. Merely claiming nonfunctional descriptive material stored in a computer-readable medium does not make it statutory. Such a result would exalt form over substance. In re Sarkar, 588 F.2d 1330, 1333, 200 USPQ 132, 137 (CCPA 1978) ("[E]ach invention must be evaluated as claimed; yet semantogenic considerations preclude a determination based solely on words appearing in the claims. In the final analysis under 101, the claimed

invention, as a whole, must be evaluated for what it is.") (quoted with approval in Abele, 684 F.2d at 907, 214 USPQ at 687). See also In re Johnson, 589 F.2d 1070, 1077, 200 USPQ 199, 206 (CCPA 1978) ("form of the claim is often an exercise in drafting"). Thus, nonstatutory music is not a computer component and it does not become statutory by merely recording it on a compact disk. Protection for this type of work is provided under the copyright law.

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claim 1, 61,62,63,64 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1,2 ,3,4,5 of U.S. Patent No. 6,266,758. Although the conflicting claims are not identical, they are not patentably distinct from each other because while claim 1 of the current application recite additional feature of "the first vector contains a first byte of an aligned vector to be generated" than the patented claim 1, it would have been obvious to one of ordinary skill in the art to recognize the first vector was capable of containing the first byte of the

aligned vector based on the step of determining a starting byte in the first register which specified the first byte of the aligned vector (see determining steps in both cases in claims 1), and because the general feature (patented claim 1) of determining the starting byte, which specified the first byte in the aligned vector, would be applicable to any specific vector, such as first or N-the vector, loaded into the first register in order to enhance the adaptability of predefined set of vector length, and for doing so, provided a motivation (see the loading of first vector in first register in claim 1 lines 7 of current case). Claims 61, 62,63,64 included limitations of claim 1 and includes also the same feature recited in patented claims 2,3,4,5, respectively.

5. Claims 1, 59-60 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 , 3-9 of U.S. Patent No. 5,933,650. Although the conflicting claims are not identical, they are not patentably distinct from each other because while the current claim 1 recites the additional feature of the starting byte is specified as a constant in alignment instruction" than the patented claim 1, it would have been obvious to one of ordinary skill in the art to specify the starting byte as a constant because the patented claim 1 generally encompassed any type of starting byte, such as variable or constant and one of ordinary skill in the art should be able to use either a variable or a constant in the first byte based on these two only choices available in the art (i.e. either fixed or variable) at the time the claimed invention was made in order to increase the ability to adjust to different requirements of

the instruction width . Claims 59-60 included limitations of claim 1 and recites the same feature as patented claims 3-9.

6. Claim 52 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 6 of U.S. Patent No. 6,266,758. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 6 additionally included computer system including a processor having plurality of registers, and claim 52 is generic to the species of invention covered by claim 6 of the patent. Thus, the generic invention is "anticipated" by the species of the patented invention. Cf., Titanium Metals Corp. v. Banner, 778 F.2d 775, 227 USPQ 773 (Fed. Cir. 1985) (holding that an earlier species disclosure in the prior art defeats any generic claim) . This court's predecessor has held that, without a terminal disclaimer, the species claims preclude issuance of the generic application. In re Van Ornum, 686 F.2d 937, 944, 214 USPQ 761, 767 (CCPA 1982); Schneller , 397 F.2d at 354. Accordingly, absent a terminal disclaimer, claim 52 is properly rejected under the doctrine of obviousness-type double patenting (see In re Goodman (CA FC) 29 USPQ2d 2010).

7. Claim 53 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 6 of U.S. Patent No. 6,266,758. Although the conflicting claims are not identical, they are not patentably distinct from each other because while patented claim 6 did not specifically show the elements written inn third register comprise the target vector as claimed in the current claim , it would have been obvious to one of ordinary skill in the art to include a target vector in

the third register because one of ordinary skill in the art should be able to recognize the first and second N-bit vectors could be designated as either a destination vector or source vector in order to facilitate the SIMD operation, and hence provided a motivation.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1,49,52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal et al. (5,887, 183) in view of Cho et al. (5,922,066).

As to claim 1, Agarwal disclosed a system (fg.4A) comprising at least :

a) loading a first vector (XJ from a memory into a vector register (see fg.4A; see col. 13, lines 13-50, see also fg.6A col. 1 1, lines 46-50 for real and imaginary elements in respective registers, and the loading of even and odd number vector elements in col. 13, lines 10-25),.

B) loading a second vector (X+1j) into a second register (see the subsequent vector loading in fg.4A; see col. I 3, lines 13-50),.

c) determination a starting byte (32 bits) in a first register wherein the starting byte specifies the first byte (32) of an aligned vector (64 bit, see the use of byte or word col. 15, lines 15-30, see also the aligned vector in col. 15, lines 31-67, col. 16, lines 1-14),.

d) extracting a first width vector (64 bit) from a first register beginning from the first bit (higher/lower bit) continuing through a bit in second register (e.g. see the consecutive single precision elements in col.15, lines 44-50).

9. Agarwal did not specifically show the replication of the art width vector into a third register as claimed. However, Cho disclosed a system including replicating a first width vector (vector operand into a third register (resultant vector register) (e.g. see the shifting into the resultant vector in co1.5, lines 14-20). It would have been obvious to one of ordinary skill in the art to use Cho in Agarwal for replicating the extracted vector into the third register as claimed because the use of Cho could provide predetermined vector format, such as aligned vector, for given operation, such as read/write, at particular word length in the execution of the instruction sequence, and it could be readily done by selecting partial vectors, such as word , or byte, of the data elements into a newly aligned vector register in Agarwal.

10. As to claim 49, Agarwal disclosed at least :

a) loading a first vector (X) from a memory into a vector register (see fg.4A; see col. 13, lines 13-50 , see also fig.6A, col. 1 1, lines 46-50 for real and imaginary elements in respective registers and the loading of even and odd number vector elements in col. 13, lines 10-25),

b) loading a second vector (X+1q into a second register (see the subsequent vector loading in fig.4A; see col. 13, lines 13-50), clearing a first plurality of elements (W11) from a first register (260) and second plurality of elements (Vri+1) from a second registerlz6z) (see col. 1 1, lines 56-67, col.12, lines 1-10).

11. Agarwal did not specifically show the writing of the first plurality of elements and second plurality of elements into a third register in particular order as claimed. However, Cho disclosed a system including writing a first plurality of elements (vector operand AJ and second plurality of elements (vector operand B1 into a third register (resultant vector register) (e.g. see the Ring into the resultant vector in col.5, lines 14-20). It would have been obvious to one of ordinary skill in the art to use Cho in Agarwal for writing the first and second into the third register as claimed because the use of Cho could enhance the control of a predetermined vector format, such as aligned vector, for a given processing, such as read/write, at specific word width in the operation of the execution of the instruction sequence, and it could be readily achieved by selecting partial vector elements, such as word , or byte, of the data vector into a newly aligned vector register in Agarwal.

12. As to claim 52, Agarwal disclosed at least :

a) loading a first source vector (X) from a memory into a vector register (see fg.4A; see col. 13, lines 13-50 , see also fg.6Aa col. 1 1, lines 46-50 for real and imaginary elements in respective registers and the loading of even and odd number vector elements in col. 13, lines 10- 25),.

b) loading a second source vector (X+1) into a second register (see the subsequent vector loading in fg.4A; see col. 13, lines 13-50,see also fg.6A, col.l 1, lines 46-50 for real and imaginary elements in respective registers and the loading of even and odd number vector elements in col. 13, lines 10-25).

Agarwal did not specifically show the selection of the first subset of element and the selection of the second subset of elements comprising the combination of odd, even, lower or upper as claimed. instead Agarwal disclosed only a combination of even and odd subset of data elements (see col. 13, lines 10-25). However, Cho disclosed an input selection circuit (310) for selecting a first and a second data elements (see col.5, lines 1 1-20). It would have been obvious to one of ordinary skill in the art to use Cho in Agarwal for selecting the first and second plurality of elements as claimed because the use of Cho could increase the flexibility of loading the vector elements to accept to different order of the input vector, such as even or odd data elements, at a specific sequence of the input vectors, and it could be done by inserting a selector into the vector register interface unit of Agarwal to adaptively select the either the first or second vectors from the vector registers.

13. The following are effective only if the "101" and Double Patenting rejections were solved :

14. Claims 50, 51 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record specifically further recite the combined features of writing even-numbered, lower elements of said

first register to said third register', writing sign bits of odd-numbered, lower elements of said first register to the third register (claim 50), and writing even-numbered, upper elements of said first register to said third register; and writing sign bits of odd numbered, upper elements of said first register to the third register (claim 51).

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Gallup et al. (5,537,562) is cited for the teaching of the 64 bit vector length in SIMD (see col.24, lines 32-68, col.25, lines 1-15, see also fig.2-7).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

DANIEL H. PAN
PRIMARY EXAMINER
GROUP